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**APPLICATION FOR LETTERS PATENT**

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**INTEGRATED CIRCUITRY AND METHODS OF  
FORMING CIRCUITRY**

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# INTEGRATED CIRCUITRY AND METHODS OF FORMING CIRCUITRY

## TECHNICAL FIELD

This invention pertains to semiconductive processing methods of forming integrated circuitry, as well as to semiconductive device circuitry.

## BACKGROUND OF THE INVENTION

A common method of forming memory devices is to form an array of devices (a so-called memory array), and to form control devices at a periphery of the array. The memory array can comprise, for example, a dynamic random access memory (DRAM) array comprising arrays of capacitors and transistors. The peripheral circuitry can comprise, for example, transistors. Frequently, the memory array circuitry and the peripheral circuitry will be covered by insulative materials. Conductive contact plugs can be formed to extend through the insulative materials to electrically connect peripheral circuitry and memory array circuitry to one another, or to other circuitry.

A continuing goal in semiconductor device fabrication is to minimize process steps. Accordingly, it would be desired to develop processing methods which reduce processing steps associated with forming memory array circuitry and peripheral circuitry.

## SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of forming circuitry. A capacitor electrode is formed over one region of a substrate and a conductive diffusion barrier layer is formed proximate the electrode. A dielectric layer is formed. The diffusion barrier layer is between the electrode and the dielectric layer. A conductive plug is formed over another region of the substrate. The conductive plug comprises a same material as the conductive diffusion barrier layer and at least a portion of the conductive plug is formed simultaneously with the conductive diffusion barrier layer.

In another aspect, the invention encompasses an integrated circuit comprising a capacitor and a conductive plug wherein the conductive plug and capacitor include a common and continuous layer.

In yet another aspect, the invention encompasses a circuit construction. The circuit construction includes a substrate having a memory array region and a region that is peripheral to the memory array region. The circuit construction also includes a capacitor construction over the memory array region of the substrate. The capacitor construction comprises a storage node, a dielectric layer and a cell plate layer. The dielectric layer is between the storage node and the cell plate layer. The circuit construction further includes an electrical interconnect over the peripheral region. The interconnect is

1 electrically connected to the cell plate layer and extends between the cell  
2 plate layer and the substrate.

### 3 4 BRIEF DESCRIPTION OF THE DRAWINGS

5 Preferred embodiments of the invention are described below with  
6 reference to the following accompanying drawings.

7 Fig. 1 is a fragmentary, diagrammatic, cross-sectional view of a  
8 semiconductive wafer fragment at a preliminary processing step of a  
9 method of the present invention.

10 Fig. 2 is a view of the Fig. 1 wafer fragment shown at a  
11 processing step subsequent to that of Fig. 1.

12 Fig. 3 is a view of the Fig. 1 wafer fragment shown at a  
13 processing step subsequent to that of Fig. 2.

14 Fig. 4 is a view of the Fig. 1 wafer fragment shown at a  
15 processing step subsequent to that of Fig. 3.

16 Fig. 5 is a view of the Fig. 1 wafer fragment shown at a  
17 processing step subsequent to that of Fig. 4.

18 Fig. 6 is a view of the Fig. 1 wafer fragment shown at a  
19 processing step subsequent to that of Fig. 5.

20 Fig. 7 is a view of the Fig. 1 wafer fragment shown at a  
21 processing step subsequent to that of Fig. 6.

22 Fig. 8 is a view of the Fig. 1 wafer fragment shown at a  
23 processing step subsequent to that of Fig. 7.

1 Fig. 9 is a view of the Fig. 1 wafer fragment shown at a step  
2 subsequent to that of Fig. 6 in accordance with a second embodiment  
3 method of the present invention.

4 Fig. 10 is a view of the Fig. 9 wafer fragment shown at a step  
5 subsequent to that of Fig. 9.

6 Fig. 11 is a view of the Fig. 1 wafer fragment shown at a step  
7 subsequent to that of Fig. 3 in accordance with a third embodiment  
8 method of the present invention.

9 Fig. 12 is a view of the Fig. 11 wafer fragment shown at a  
10 processing step subsequent to that of Fig. 11.

11 Fig. 13 is a view of the Fig. 1 wafer fragment shown at a  
12 processing step subsequent to that of Fig. 6 in accordance with a fourth  
13 embodiment method of the present invention.

14 Fig. 14 is a view of a semiconductive wafer fragment shown at a  
15 processing step subsequent to that of Fig. 2 in accordance with a fifth  
16 embodiment method of the present invention.

17 Fig. 15 is a view of the Fig. 14 wafer fragment shown at a  
18 processing step subsequent to that of Fig. 14.

19 Fig. 16 is a view of the Fig. 14 wafer fragment shown at a  
20 processing step subsequent to that of Fig. 15.  
21  
22  
23

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

In one aspect, the present invention encompasses a recognition that processing steps associated with the formation of circuitry over a memory array region of a semiconductive wafer substrate can be consolidated with processing steps associated with formation of circuitry over a peripheral region of the substrate. Such will become more apparent with reference to Figs. 1-6, which illustrate initial processing of a method of the present invention.

Referring initially to Fig. 1, a semiconductor wafer fragment 10 comprises a semiconductive substrate 12. Substrate 12 can comprise, for example, a monocrystalline silicon wafer lightly doped (i.e., doped to a concentration of less than or equal to about  $10^{16}$  atoms/cm<sup>3</sup>) with a p-type dopant. To aid in interpretation of the claims that follow, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described

1 above. Semiconductive substrate 12 comprises a memory array region 14  
2 and a peripheral region 16.

3 Word lines 18, 20 and 22 are formed over substrate 12. Word  
4 lines 18, 20 and 22 comprise a gate stack 24 and sidewall spacers 26.  
5 Gate stack 24 can comprise, for example, layers of silicon dioxide,  
6 polysilicon and silicide. Sidewall spacers 26 can comprise, for example,  
7 silicon nitride or silicon oxide.

8 Field oxide regions 28 are formed over substrate 12 within memory  
9 array region 14. Field oxide regions 28 can comprise, for example,  
10 silicon dioxide.

11 Electrical nodes 30 and 32 are defined adjacent word line 18, and  
12 electrical nodes 34, 36 and 38 are defined adjacent word lines 20  
13 and 22. Wordlines 18, 20 and 22 can comprise transistors, and  
14 nodes 30, 32, 34, 36 and 38 can comprise source/drain regions of such  
15 transistors. Nodes 30 and 32 are proximate peripheral region 16 of  
16 substrate 12. The term "proximate" indicates that nodes 30 and 32 can  
17 be within, above or below peripheral region 16 of substrate 12  
18 (embodiments in which nodes are elevationally displaced from  
19 substrate 12 are not shown). Similarly, nodes 34, 36 and 38 are  
20 proximate memory array region 14 of substrate 12. Nodes 30, 32, 34,  
21 36 and 38 can comprise, for example, conductive diffusion regions formed  
22 within substrate 12. Such diffusion regions can be formed by, for  
23 example, implanting conductivity-enhancing dopant into substrate 12.

1 An electrically insulative layer 40 is formed over substrate 12, and  
2 over word lines 18, 20 and 22. Insulative layer 40 can comprise, for  
3 example, borophosphosilicate glass (BPSG), and can be formed by, for  
4 example, chemical vapor deposition.

5 Referring to Fig. 2, openings 42 and 44 are etched through  
6 insulative layer 40 to nodes 34 and 38, respectively. Openings 42  
7 and 44 can be formed by, for example, providing a photoresist mask (not  
8 shown) over layer 40, and patterning the mask to expose regions of  
9 insulative layer 40 at opening locations 42 and 44. Insulative layer 40  
10 can then be etched with, for example, a fluorine-containing plasma to  
11 form openings 42 and 44. The photoresist mask can be subsequently  
12 removed to leave the structure shown in Fig. 2.

13 Referring to Fig. 3, capacitor storage nodes 46 and 48 are formed  
14 within openings 42 and 44 (Fig. 2), respectively. Capacitor storage  
15 nodes 46 and 48 can comprise, for example, polysilicon and preferably  
16 comprise the shown roughened outer surfaces 50 and 52. Such  
17 roughened outer surfaces can be formed by, for example, deposition of  
18 hemispherical grain polysilicon.

19 A dielectric layer 54 is formed over storage nodes 46 and 48.  
20 Dielectric layer 54 can comprise, for example, one or more of silicon  
21 dioxide or silicon nitride, and preferably comprises tantalum oxide.  
22 Dielectric layer 54 can be formed by, for example, chemical vapor  
23 deposition. Storage nodes 46 and 48, and dielectric layer 54, can be



1 formed by methods known to persons of ordinary skill in the art, such  
2 as, for example, chemical vapor deposition. In the shown embodiment,  
3 the material of storage nodes 46 and dielectric layer 54 does not extend  
4 over peripheral region 16. Such can be accomplished by, for example,  
5 masking peripheral region 16 while forming nodes 46 and 48, and while  
6 forming dielectric layer 54.

7 Referring to Fig. 4, a photoresist masking layer 56 is provided over  
8 regions 14 and 16 of substrate 12 and patterned to define openings 58  
9 and 60 in peripheral region 16.

10 Referring to Fig. 5, openings 58 and 60 are extended to node  
11 locations 30 and 32, respectively. Openings 58 and 60 can be extended  
12 by, for example, a plasma etch utilizing a fluorine-containing component.

13 Referring to Fig. 6, photoresist material 56 (Fig. 5) is removed.  
14 Subsequently, a conductive material 62 is formed over both peripheral  
15 region 16 and memory array region 14 of substrate 12. In the shown  
16 embodiment, conductive material 62 comprises two separate layers (64  
17 and 66). Layer 64 can comprise, for example, a metal nitride, such as  
18 titanium nitride or tungsten nitride, and layer 66 could comprise a metal  
19 such as tungsten, aluminum or copper. The metal of layer 66 can be  
20 in either an elemental form, or in the form of an alloy, such as  
21 aluminum/copper. Layers 64 and 66 can be formed by, for example,  
22 chemical vapor deposition and/or sputter deposition.  
23

1           Layers 64 and 66 would typically have different functional purposes  
2 at peripheral region 16 relative to memory array region 14. Specifically,  
3 layers 64 and 66 form contact plugs 65 and 67 at peripheral region 16,  
4 with layer 64 preferably comprising a metal nitride and functioning as  
5 an adhesive layer for adhering metal layer 66 within openings 58 and 60  
6 (Fig. 5). Layer 64 can also function to prevent diffusion of dopant from  
7 diffusion regions 30 and 32 into metal layer 66. In contrast, layers 64  
8 and 66 form at least a portion of a capacitor electrode 81 over memory  
9 array region 14. Specifically, layers 64 and 66 together define at least  
10 a portion of capacitor cell plate 81, with conductive material 62 and  
11 dielectric layer 54 being operatively adjacent storage node layers 46  
12 and 48 to form capacitor structures 70 and 72. In embodiments in  
13 which dielectric layer 54 comprises tantalum oxide, layer 64 preferably  
14 comprises a metal nitride. Layer 64 can then function as a capacitor  
15 diffusion barrier layer to inhibit undesired diffusion of materials between  
16 tantalum oxide layer 54 and upper capacitor electrode layer 66.

17           Although material 62 is shown as comprising two layers, it is to  
18 be understood that the invention also encompasses embodiments in which  
19 material 62 comprises only one layer, and other embodiments in which  
20 material 62 comprises more than two layers. For instance, material 62  
21 can comprise three layers wherein a first layer is titanium deposited to  
22 form titanium silicide at the bottoms of openings 58 and 60 (Fig. 5),  
23

1 and the remaining two layers are a metal nitride layer (such as TiN)  
2 and a metal layer (such as Al).

3 In the shown embodiment, conductive material layer 62 is formed  
4 over peripheral region 16 and memory array region 14 in a common  
5 deposition step. Thus, such embodiment consolidates formation of  
6 conductive contact plugs 65 and 67 with formation of capacitor  
7 electrode 81 over memory array region 14. Such can save process steps  
8 relative to prior art methods which form conductive contacts over a  
9 peripheral region of a substrate separately from formation of a capacitor  
10 electrode over a memory array region of the substrate.

11 Figs. 7-10 illustrate alternative processing methods which can be  
12 utilized for patterning conductive material at peripheral region 16.  
13 Figs. 7-8 illustrate a first embodiment method, and Figs. 9-10 illustrate  
14 a second embodiment method. Referring first to the embodiment of  
15 Figs. 7 and 8, and specifically referring first to Fig. 7, a photoresist  
16 masking layer 76 is provided over memory array region 14 while leaving  
17 peripheral region 16 exposed to an etching process. The etch process  
18 removes conductive material 62 from over insulative material 40 at  
19 peripheral region 16 to electrically isolate conductive plugs 65 and 67  
20 from one another.

21 Referring to Fig. 8, a conductive layer 80 is formed over memory  
22 array region 14 and peripheral region 16 and patterned to form isolated  
23 electrical contacts with conductive plugs 65 and 67, and to form another

1 portion of capacitor electrode 81 for capacitor constructions 70 and 72.  
2 More specifically, layer 80 and conductive material 62 together form  
3 capacitor electrode 81 for capacitors 70 and 72. Conductive layer 80 can  
4 comprise, for example, a metal such as tungsten, titanium, copper and/or  
5 aluminum, and can be formed by, for example, sputter deposition.  
6 Alternatively, conductive layer 80 can comprise a conductively doped  
7 semiconductive material, such as, for example, conductively doped  
8 polysilicon. Subsequent processing (not shown) such as provision of an  
9 interlevel dielectric or spin-on-glass over one or both of regions 14 and  
10 16, followed by chemical-mechanical planarization can be conducted to  
11 form an insulative layer over regions 14 and 16.

12 Referring to the embodiment of Figs. 9 and 10, identical  
13 numbering to that utilized in describing the embodiment of Figs. 7 and 8  
14 will be used. A difference between the embodiment of Figs. 9 and 10  
15 and that of Figs. 7 and 8 is that in the Fig. 9 and 10 embodiment  
16 conductive material 80 is formed over memory array region 14 and  
17 peripheral region 16 prior to etching of conductive material 62.

18 Referring initially to Fig. 9, conductive layer 80 has been formed  
19 over memory array region 14 and peripheral region 16.

20 Referring to Fig. 10, conductive layer 80 and conductive  
21 material 62 are patterned in a common etch to electrically isolate  
22 conductive plugs 65 and 67 from one another, and to electrically isolate  
23 the circuitry of peripheral region 16 from that of memory array

1 region 14. The patterning of material 62 and layer 80 can comprise, for  
2 example, formation of a patterned photoresist layer (not shown) over  
3 layer 80, and subsequent transferring of a pattern from the photoresist  
4 layer to underlying layer 80 and conductive material 62 to form the  
5 structure shown in Fig. 10. The patterned photoresist layer forms a  
6 protective layer over a portion of conductive material 80 that is over  
7 storage nodes 46 and 48 that protects such portion of conductive  
8 material 80 as another portion of conductive material 80 is removed from  
9 over peripheral region 16. The portion of conductive material 80  
10 removed from peripheral region 16 is proximate to where openings 58  
11 and 60 (Fig. 5) were formed.

12 Another embodiment of the invention is described with reference  
13 to Figs. 11 and 12. In describing to Figs. 11 and 12, identical  
14 numbering to that utilized above in describing Figs. 1-10 will be used,  
15 with differences indicated by different numerals.

16 Referring first to Fig. 11, semiconductive wafer fragment 10 is  
17 shown at a processing step subsequent to that of Fig. 3, with a layer 90  
18 formed over dielectric layer 54 in memory array region 14, and extending  
19 to over peripheral region 16. Layer 90 can comprise, for example, a  
20 diffusion barrier layer such as, for example, titanium nitride or tungsten  
21 nitride.

22 Referring to Fig. 12, openings are formed through layer 90 and to  
23 node locations 30 and 32, and subsequently filled with conductive

1 material 62. The formation of the openings and subsequent filling of  
2 such openings with conductive material 62 can occur through processing  
3 similar to that described with reference to Figs. 4-6. Wafer fragment 10  
4 of Fig. 12 can then be subjected to subsequent processing analogous to  
5 that of either the embodiment of Figs. 7-8 or the embodiment of  
6 Figs. 9-10 to form isolated conductive plugs in electrical contact with  
7 node locations 30 and 32, and to form capacitor structures similar to the  
8 structures 70 and 72 of Figs. 8 and 10.

9 Yet another embodiment of the present invention is described with  
10 reference to Fig. 13 which illustrates a semiconductive wafer fragment 10  
11 at a processing step subsequent to that of Fig. 9. In the Fig. 13  
12 embodiment, conductive layer 80 and conductive material 62 are  
13 patterned to electrically isolate contact plugs 65 and 67 from one  
14 another, but contact plug 67 remains in electrical connection with the  
15 upper capacitor electrode 81 over memory array region 14. Thus  
16 layers 64 and 66 are common and continuous layers comprised by both  
17 contact plug 67 and capacitors 70 and 72. In the Fig. 13 embodiment,  
18 contact plug 67 forms an electrical connection between memory array  
19 region 14 and electrical node 32.

20 The embodiment of Fig. 13 can be advantageous over prior art  
21 methods for providing a good electrical contact to a cell plate electrode.  
22 Specifically, prior art methods utilize electrical connects extending  
23 upwardly from a cell plate layer. Such electrical connects are formed

1 by providing an insulative layer over the cell plate layer and etching  
2 downwardly through the insulative layer to expose the cell plate layer.  
3 Occasionally, the etch extends through the cell plate layer and results in  
4 a poor electrical connection to the cell plate layer. In contrast, the  
5 embodiment of Fig. 13 utilizes an electrical connection extending  
6 downwardly from a cell plate layer and formed during formation of the  
7 cell plate layer. Specifically, at least a portion of the cell plate layer 81  
8 is preferably formed over electrical interconnect 67 during formation of  
9 electrical interconnect 67.

10 It is noted that the invention also encompasses embodiments  
11 wherein cell plate layer 81 from memory array region 14 extends to  
12 physically contact more than one contact plug in peripheral region 16.  
13 Such embodiments can provide redundancy in the event that one or  
14 more of the connections fails. In the shown embodiment,  
15 interconnects 65 and 67 are connected through a switch comprising word  
16 line 18. Interconnect 65 can then be connected to other circuitry (not  
17 shown) to provide a switchable connection between such other circuitry  
18 and the capacitor plate 81 over memory region 14.

19 Yet another embodiment of the present invention is described with  
20 reference to Figs. 14-16. In describing the embodiment of Figs. 14-16,  
21 identical numbering to that utilized above in describing the embodiments  
22 of Figs. 1-13 will be used, with differences indicated by different  
23 numerals.

1 Referring to Fig. 14, wafer fragment 10 is illustrated at a  
2 processing step subsequent to that of Fig. 2. Specifically, storage  
3 nodes 46 and 48 are formed within openings 42 and 44 (Fig. 2). Wafer  
4 fragment 10 of Fig. 14 differs from the wafer fragment 10 of Fig. 3  
5 (which is also at processing step subsequent to that of Fig. 2) in that  
6 there is no dielectric layer 54 provided over storage nodes 46 and 48 in  
7 the embodiment of Fig. 14.

8 Fig. 15 illustrates the wafer fragment 10 of Fig. 14 after it has  
9 been subjected to processing analogous to that described above with  
10 reference to Figs. 4-6. Specifically, a conductive material 62 has been  
11 formed over storage nodes 46 and 48. Conductive material 62 has also  
12 been formed in electrical contact with node locations 32 to form  
13 electrical interconnects 65 and 67 over peripheral region 16 of  
14 substrate 12. As there was no dielectric layer formed prior to provision  
15 of conductive material 62, material 62 electrically interconnects with  
16 nodes 46 and 48 to effectively become a portion of the capacitor storage  
17 nodes 46 and 48.

18 A patterned photoresist layer 100 is provided over peripheral  
19 region 16 and memory array region 14. Patterned photoresist layer 100  
20 has openings 102 extending through it.

21 Referring to Fig. 16, openings 102 (Fig. 15) are extended to  
22 electrically isolate electrical interconnects 65 and 67 from one another  
23 and from memory array region 14, as well as to electrically isolate



1 storage nodes 46 and 48 from one another. Photoresist layer 100 (Fig.  
2 15) is then removed, and a dielectric layer 54 is formed over memory  
3 array region 14. Dielectric layer 54 can be formed by, for example,  
4 processing described above with reference to Fig. 3. After formation of  
5 dielectric layer 54, a conductive layer 80 is provide over storage  
6 nodes 46 and 48, as well as over electrical interconnects 65 and 67.  
7 Conductive material 80 is then patterned to form a cell plate 81 over  
8 storage nodes 46 and 48, and to form electrically isolated contacts to  
9 interconnects 65 and 67. The formation and patterning of layer 80 can  
10 be conducted in accordance with the methods described above in  
11 reference to Figs. 7 and 8.

12 The embodiment of Figs. 14-16 forms a diffusion barrier layer 64  
13 that is part of capacitor storage nodes 46 and 48. In the shown  
14 embodiment, material 62 can comprise diffusion barrier components  
15 throughout its thickness. Specifically, layers 64 and 66 can both  
16 comprise either titanium nitride or tungsten nitride.

17 It is noted that the embodiments described above form a diffusion  
18 barrier layer as either part of a storage node, or as a part of a  
19 capacitor plate. The invention encompasses other embodiments (not  
20 shown) wherein one or more of the above-described embodiments are  
21 combined to form a diffusion barrier region as part of a storage node  
22 and to also form a diffusion barrier region as part of a capacitor plate.  
23

1           It is also noted that there will typically be a bit line contact (not  
2 shown) formed in electrical connection with node 36 in the embodiments  
3 described above to connect node 36 to a bit line (not shown). Such bit  
4 line can be either above the capacitors (a so-called capacitor over bit  
5 line construction) or beneath at least a portion of the capacitors (a so-  
6 called capacitor over bit line construction).

7           In compliance with the statute, the invention has been described  
8 in language more or less specific as to structural and methodical  
9 features. It is to be understood, however, that the invention is not  
10 limited to the specific features shown and described, since the means  
11 herein disclosed comprise preferred forms of putting the invention into  
12 effect. The invention is, therefore, claimed in any of its forms or  
13 modifications within the proper scope of the appended claims  
14 appropriately interpreted in accordance with the doctrine of equivalents.